Multi-condition alternate test of analog, mixed-signal, and RF systems

Manuel J. Barragan, Gildas Leger, and Jose L. Huertas
Instituto de Microlectrónica de Sevilla, Centro Nacional de Microelectrónica
Consejo Superior de Investigaciones Científicas (CSIC) and Universidad de Sevilla
Av. Américo Vespucio s/n, 41092 Sevilla, Spain.
e-mail: manuelj@imse-cnm.csic.es

***Abstract*—This work proposes a generic path to improve Alternate Test strategies. It demonstrates that multi-condition test increases the amount of information present in the test data and consequently decreases the prediction error of the trained models. The ambition of this paper is to be a methodological contribution to the field of AMS-RF test, and formal guidelines are provided that justify the interest of the approach. For the sake of validation, the proposed methodology has been applied to several alternate test strategies for analog, mixed signal, and RF circuits. Promising results are found for the following case studies: an analog filter, a $\Sigma\Delta$ A/D converter, and an RF LNA.**

I. Introduction

Nowadays, commercial trends of IC industry have forced the integration of complex SoCs consisting of tightly integrated analog, mixed-signal, RF and digital circuitry onto a single IC substrate. This high integration level provides a significant reduction in production cost, but there is a simultaneous increase in the cost of testing and diagnosing these devices.

Usually, the main test difficulties are due to the test of non-digital parts. Analog, mixed-signal and RF testing are usually based on functional characterization, while fault-model-based tests, very successful in the digital test domain, are difficult to standardize in the non-digital field since each circuit type demands its own custom fault model.

Alternate test has been proposed as a promising solution to mitigate most non-digital test drawbacks [1]. These strategies take advantage of advanced statistical tools to find correlations between a number of observables (signatures), and the diverse DUT specifications. The main interest resides in the fact that these signatures can be much cheaper to generate than the specification measurements.

Unfortunately for the industry, no clear path for a systematic (and automatic) test approach is being devised. Knowledge and experience are still needed to propose the best input space to feed these statistical tools. Thus, finding an appropriate set of signatures to extract meaningful models is usually a matter of creativity based on a precise knowledge of the DUT. In this line, the work in [2] explores the use of a simple multi-V_{DD} technique to improve the accuracy of RF alternate test at almost no extra engineering cost. This paper extends this multi-V_{DD} technique to a generalized multi-condition strategy. This multi-condition strategy takes advantage of the variation of the DUT performance under multiple operating conditions to add extra layers of information to the input space of observables. The feasibility of the proposed technique is demonstrated in the analog, mixed-signal, and RF test domains by its direct application to three different test strategies for analog filters, $\Sigma\Delta$ A/D converters, and RF LNAs, previously published by the authors [3]–[5].

This paper is organized as follows. Section II describes the theoretical basis of our proposal. Then Section III presents case studies in the analog, mixed signal, and RF domains. Section IV discusses some relevant experimental results to validate the proposal. Finally, Section V summarizes the main contributions of this work.

II. Theoretical basis: Alternate test under multiple operating conditions

Testing a circuit under multiple conditions is not new. Even during its design stage a circuit is simulated under different power supplies, V_{DD}, to assure its functionality in the technology process corners. The use of Multi-V_{DD} and V_{DD} ramping have been also explored as a reliable way of detecting defects in analog and RF circuits [6], and supply voltage modulation has been used to achieve better testing of opamps [7]. This proposal demonstrates that performing classical alternate test strategies under multiple operating conditions such as different power supplies, different working frequencies, etc, has the potential to significantly improve the accuracy of alternate test results at a low added cost.

Let us consider the set of performance specifications, $\mathbf{p} = [p_1, p_2, ..., p_k]$, of a certain DUT, and let $\mathbf{s} = [s_1, s_2, ..., s_m]$ be a set of signatures corresponding to the same DUT, where $\mathbf{p}$, and $\mathbf{s}$ belong to the space of possible specification sets, P^k, and to the space of possible signature sets, S^m, defined by process variations, respectively. Alternate test strategies use statistical processing to find a mapping function f defined as $f : S^m \longrightarrow P^k$ that verifies:

$$\|f(\mathbf{s}) - \mathbf{p}\| \rightarrow 0 \tag{1}$$

for each $\mathbf{s} \in S^m$ and $\mathbf{p} \in P^k$. Let us assume as hypothesis that such a function f exists, and let us now consider the measurement of the set of observables $\mathbf{s}$ under a different operating condition X. In a first order approximation, the variation will affect each signature in $\mathbf{s}$ as,

$$s_{i\Delta} \simeq s_i + \frac{\partial s_i}{\partial X}\Delta X \tag{2}$$

where $s_{i\Delta}$ corresponds to signature s_i measured under operating condition $X + \Delta X$, and X is the nominal operating condition. Equation (2) can be expanded as,

$$s_{i\Delta} \simeq s_i + \sum_{j=1}^{k} \frac{\partial s_i}{\partial p_j}\frac{\partial p_j}{\partial X}\Delta X \tag{3}$$

Given that the $k \times m$ matrix $\left[\frac{\partial s_i}{\partial p_j}\right]$ has to be different from the $k \times m$ null matrix by our initial hypothesis (that is, mapping function f exists), in the case that the sensitivity vector $\left[\frac{\partial p_1}{\partial X}, ..., \frac{\partial p_k}{\partial X}\right]$ is different from the null vector, then signature set $\mathbf{s_\Delta} = [s_{1\Delta}, ..., s_{m\Delta}]$ contains functional information about the sensitivity of the DUT specifications to changes in operating condition X.

Let S^m_Δ be the space of possible signature sets defined by process variations and measured under operating condition $X + \Delta X$. Space S^m_Δ can be used to complement the functional information about the DUT contained in S^m in such a way that a new mapping function, f_Δ, can be defined as $f_\Delta : S^m \cup S^m_\Delta \longrightarrow P^k$. If we compare mapping functions f and f_Δ, given that the space of observables $S^m \cup S^m_\Delta$ contains more information about the DUT behavior than the space S^m alone, it should be clear that,

$$\|f_\Delta(\mathbf{s}, \mathbf{s_\Delta}) - \mathbf{p}\| \leq \|f(\mathbf{s}) - \mathbf{p}\| \tag{4}$$

for each $\mathbf{s}, \mathbf{s_\Delta} \in S^m \cup S^m_\Delta$ and $\mathbf{p} \in P^k$. That is, as a result of measuring under different operating conditions, the mapping model may be improved, but, interestingly, it cannot degrade. However, this development only proves the mathematical existence of a mapping function f_Δ that verifies (4) under certain assumptions (i. e. the existence of a mapping function f that verifies (1), and nonzero performance sensitivity to condition variations). Obviously, the mathematical existence of f_Δ does not guarantee the convergence of a particular machine learning algorithm to a better solution. In practice, increasing the input space dimension of machine learning algorithms is not exempt of side-effects related to the well-known curse of dimensionality. In this sense, only the signatures that provide significant additional information should be considered. Fortunately, many algorithms contemplate some form of dimensionality reduction techniques to help selecting the most relevant features.

III. Case studies

The previous discussion is completely general, and can thus be applied to any particular alternate test approach. Indeed, it has the potential to improve many already published alternate test strategies. In order to demonstrate the feasibility of this approach, we have applied it to three alternate test schemes in the analog, mixed-signal, and RF domains. This section describes briefly the alternate test schemes, selected devices under test, and the application of the proposed methodology for each particular case.

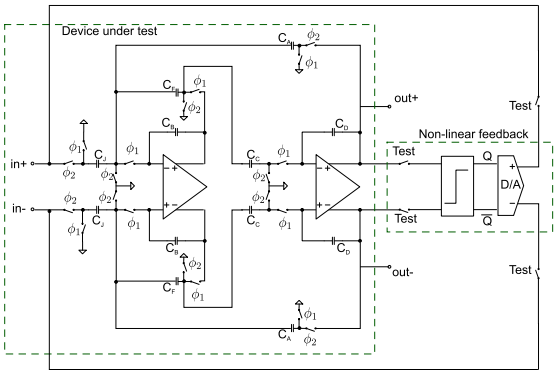

Fig. 1. Schematic of the SC filter under test

A. Analog domain: Predictive OBT of a switched-capacitor filter

1) Description of the alternate test strategy: Oscillation-based test relies in forcing oscillators either in a circuit or in a full system. The DUT is reconfigured by any means into an oscillator, and the resulting oscillation is characterized. Predictive OBT techniques build statistical models to relate characteristics of the oscillation, such as frequency, amplitude, harmonic components, etc, to performance figures of the original DUT [3], [8].

In this particular case study, we propose to use the oscillation frequency and the magnitudes of the first five harmonic components as signatures. Such set of signatures can be efficiently computed on-chip in the digital domain, and can be related to performance parameters of the DUT such as its frequency response and linearity figures. The set of signatures are processed using an Ensemble Learning model implemented using the ENTOOL Matlab toolbox [9] to extract functional information about the DUT.

2) Device under test: The selected DUT is a switched-capacitor biquad in a fully-differential lowpass configuration. Fig. 1 shows the schematic of the DUT. A non-linear feedback loop has been added to force the oscillation during the test mode. This feedback loop comprises a simple comparator followed by a single-bit D/A converter. The complete system has been designed in a 3.3V-0.35μm CMOS technology for a 1 MHz clock frequency at nominal operation conditions.

3) Application of the multi-condition strategy: In this particular case study, the predictive OBT strategy previously described is employed to estimate the THD of the filter. Thus, initially we have a 6-dimension input space (oscillation frequency and the magnitudes of the first five harmonic components) to map onto the unidimensional output space formed by the THD.

Following the analysis above, the information contained in the input space may be improved by repeating the same test at different operating conditions. A trade-off arises in the choice of this variation. On the one hand, the variation of the operating condition has to be high enough to maximize the change in the selected DUT specification, but on the other hand it has to be sufficiently low for not killing the DUT

functionality. In this particular case we propose to repeat the test at a 75% power supply, and at a ten times higher clock frequency. In this way, the dimension of the input space increases to 18.

Electrical Monte-Carlo simulations of the full schematic are used to generate the data and 4 different regression scenarios will be studied:

- the nominal input space is considered.
- the six signatures obtained for supply stress are added to the nominal ones.
- the six signatures obtained for the frequency stress are added to the nominal ones.
- the 18 previous signatures are considered.

B. Mixed-signal domain: Digital test of a 2-1 cascaded ΣΔ modulator

1) Description of the alternate test strategy: In order to validate the approach in a much different circuit, we have re-used past work on digital tests for ΣΔ converters [4]. These digital tests provide simple signatures that can be used to feed a regression model. The digital tests that are applied to the modulator have been detailed elsewhere [4], but let us briefly recall the fundamentals. The basic idea is to re-use the feedback DAC (or add an extra 1-bit DAC) to send a digital test sequence to the modulator under test. Furthermore, the modulator can be reconfigured in smaller parts such that all the integrators can be tested. The digital sequence and the DfT configuration are chosen such that the non-ideality under consideration manifests itself as a deviation in the DC component of the output bit stream. In this way, the signature can be generated with a simple counter or take advantage of the modulator decimation filter [4].

Several test signatures have been proposed but for the sake of simplicity, we only consider two of them here:

On one hand, an integrator leakage signature is obtained using a periodic sequence with mean value different from zero, and then its opposite (in order to get rid of possible offsets). More concretely the period is [1 1 1 1 1 -1] and the mean value $2/3$.

On the other hand, an integrator settling error signature is obtained with a sequence of zero mean value [1 1 -1 1 -1 -1] such that the clock period is doubled for a 1 input and remains nominal for a -1 input. Conversely, a second acquisition is performed inverting the clock dependence in order to get rid of possible offsets. For this particular test, in addition to the DC component of the output bitstream, we have to acquire the number of occurrences of the combination of a -1 input sample and a 1 feedback sample (conversely a 1 input sample and a -1 feedback sample for the second acquisition). This only requires an additional counter and a couple of logic gates.

2) Device under test: The circuit under test is the switched-capacitor third order 2-1 cascaded modulator presented in [4] and depicted in Fig. 2. Simple Design-for-Testability (DfT) modifications in the control of switches allow performing several digital tests.

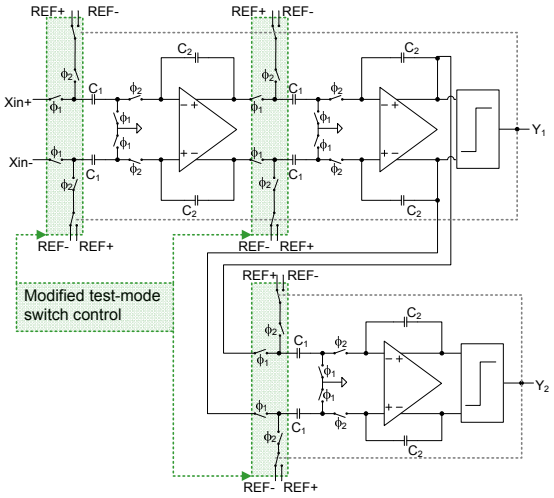

Fig. 2. Schematic of the modulator under test

3) Application of the multi-condition strategy: With the proposed DfT modifications it is actually possible to obtain the leakage and settling test signatures independently on each of the three amplifiers. Initially, we thus have a 6-dimension input space that we want to map onto the unidimensional output space formed by the SNDR.

As explained above, this input space may not contain sufficient information to obtain a good regression accuracy. As a generic way to bring more information into the regression machine, we can repeat the same tests at different supply voltages and also at different operating frequencies.

What we propose here is to repeat the six tests at 80% of the power supply. Additionally, we will also repeat the settling tests at 120% of the nominal frequency (we do not repeat the leakage tests in this case because we do not expect any change). In this way, the dimension of the input space grows to 18.

A number of 4 regression scenarios will be studied:

- the nominal input space is considered.
- the six digital signatures obtained for supply stress are added to the nominal ones.
- the three digital signatures obtained for the frequency stress are added to the nominal ones.
- the 15 previous signatures are considered.

A model is trained using Ensemble Learning for each one of these scenarios, to map the digital signatures onto the SNDR of the modulators.

Ideally, we should thus perform an electrical Monte-Carlo simulation of a ΣΔ modulator for the proposed digital tests as well as for the functional test. Unfortunately, such simulations are not feasible on our hardware because even a single simulation to measure the SNDR of an instance already takes days to complete. To circumvent this issue we instead perform a Monte-Carlo simulation of the amplifiers present in the modulator and extract their main parameters (namely, gain, output range, linearity, bandwidth, and slew-rate), at

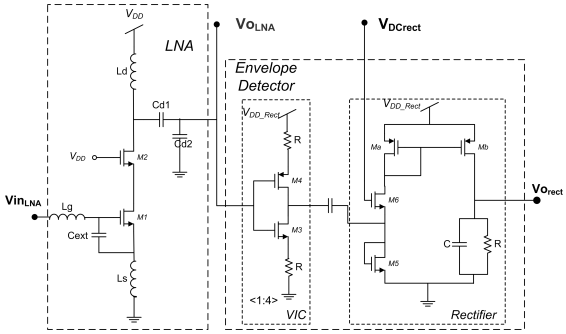

Fig. 3. Schematic of the LNA under test

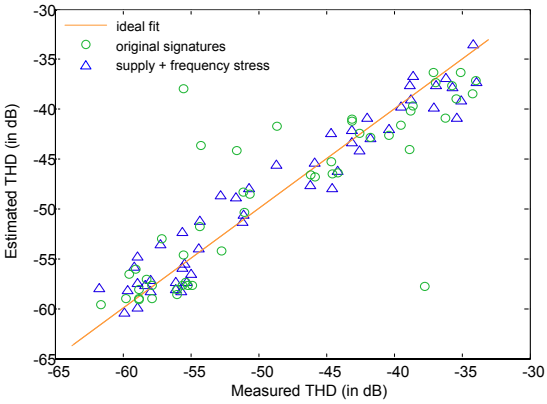

Fig. 4. Scatterplot of the regression results over the independent test set

two power supply voltages (the nominal voltage 3.3V and a reduced voltage of 2.7V). The extracted parameters are then used in a high-level model similar to those proposed in [10]. In this way, we do not have the exact details of the electrical simulation, but the correlation between the results at different power supplies is not artificial. It corresponds to real process variations. Notice that the frequency stress is applied at behavioral level directly and does not require a different Monte-Carlo simulation of the amplifiers.

C. RF domain: Alternate test of a LNA through digital envelope signatures

1) Description of the alternate test strategy: Envelope-based tests of RF blocks are based on the analysis of the low-frequency envelope of an RF signal to extract information about the original RF signal. In this particular case study we propose the analysis of a LNA response to a two-tone test stimulus. The envelope of the two-tone response signal is a low-frequency periodic function that contains information about the high frequency response of the LNA [5].

We propose the use of the area under a period of the response envelope curve as a simple test signature. Additionally, a second signature is added to compensate the variation of the envelope detector performance by bypassing the test stimulus to the detector and extracting the area under the output response. These signatures can be easily computed in the digital domain [5]. Again, ensemble learning model are used to map the obtained signatures to the DUT specifications.

2) Device under test: Our test vehicle is a LNA design that complies with the IEEE 802.15.4 standard. Fig. 3 shows the schematic of the LNA under test. The complete system has been designed in a 1.2V-90nm CMOS technology. A simple envelope detector has been included to extract the envelope of the response signals during test mode.

3) Application of the multi-condition strategy: In this particular case we initially have a 2-dimension input space that we want to map onto the 3-dimension output space defined by the Gain, Noise Figure, and 1dB-Compression Point of the LNA under test. As it was previously discussed, repeating the test under different operating conditions is a generic way to complement the information contained in the input space.

In this application example we propose to repeat the test at 90% and 110% of the power supply, so the dimension of the input space increases to 6. Two different regression scenarios will be studied: The nominal input space, and the complete input space adding the signatures obtained under stressed supplies. The data is generated by electrical Monte-Carlo simulations of the extracted layout including parasitics.

IV. Results and Discussion

A. Analog domain: Predictive OBT of a switched-capacitor filter

A set of 200 instances of the SC filter under test were obtained by electrical Monte Carlo simulation. Out of the 200 instances 150 were used to train the ensemble model, while 50 randomly chosen instances were taken apart as test set to verify the accuracy of the prediction. Model training was performed firstly under nominal conditions, and repeated in the different stressed scenarios as explained in the previous section.

Fig. 4 shows the scatterplots of the estimated THD versus the measured THD obtained for the test set when training the models with the original test signatures (circles), and for the complete set of test signatures, with both supply and frequency stress (triangles). It is clear to see the improvement in the estimation. In order to quantify this improvement we use the following Figure of Merit (FOM) for model based test, previously proposed in [5],

$$FOM = \sqrt{\frac{\sum_{i=1}^{N_s}\left(Y_{actual,i} - \bar{Y}_{actual}\right)^2}{\sum_{i=1}^{N_s}\left(Y_{pred,i} - Y_{actual,i}\right)^2}} \qquad (5)$$

where N_s is the number of tested circuits, $Y_{pred,i}$ is the performance of circuit i predicted by the model, and $Y_{actual,i}$ is the real performance of circuit i. The hat symbol stands for the mean value as usual. This FOM relates the model prediction error to the variability of the output space (i.e. the specification). It is a way to measure the information brought by the model beyond the Monte Carlo variation range. Table I shows the obtained FOM in the four considered regression scenarios. The FOM improves a significant 116% from the nominal case to the model trained with the nominal and stressed signatures. According to the obtained results it can be

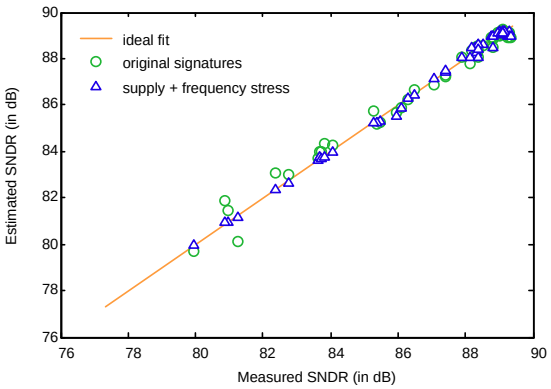

Fig. 5. Scatterplot of the regression results over the independent test set

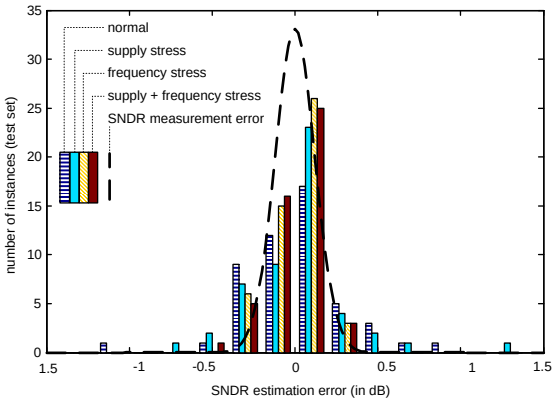

Fig. 6. SNDR estimation error for the different scenarios

conclude that frequency stress is a very good way to improve the accuracy of this Predictive OBT strategy. Power supply stress also brings an improvement, but at a lower extent. From a diagnosis point of view, it can be inferred that in terms of linearity the filter under test is much more limited dynamically (signal settling) than statically (DC gain, output range).

B. Mixed-signal domain: Digital test of a 2-1 cascaded ΣΔ modulator

A total number of 300 modulator instances have been simulated, 50 of which are set apart to form the test set. Beyond the digital tests, we also perform a traditional functional test using an input sine-wave with an amplitude of 65% of the full-scale, which corresponds to the maximum amplitude before the quantizer begins to overload (i.e. the maximum SNDR is reached). The SNDR of the modulator is calculated from the FFT of the output bit-stream. In order to obtain an accurate result, the FFT is performed over 512 points of the baseband (which for and Over-Sampling Ratio of 64 requires to simulate the modulator over 32768 samples). This measurement is repeated 10 times varying the phase of the intput sine-wave and the initial state of the integrators. The average of these spectra lead to a measurement accuracy of σ_{SNDR} = 0.1205 dB.

Fig. 5 shows the scatter plots of the estimated SNDR versus the measured SNDR obtained for the original test signatures (circles) and for the complete test set (triangles), with both supply and frequency stress. Despite the fact that the original digital tests already provide a decent fit, the estimation improvement is quite clear.

The evolution of the FOM is registered in Table I. It reaches 8.4 for the first scenario. Adding the supply stress it increases to 9.1. The original signatures plus the three signatures from the frequency stress reach a very good 17.1. And finally, the combination of frequency and supply stress only provides slight further improvement up to 17.3.

Fig. 6 displays the histograms of the estimation error in the four scenarios. In addition, the gaussian error associated to the functional SNDR measurement (whose standard deviation is 0.1205 dB) has been represented for the sake of comparison. It can be seen that the estimation error is very close to the measurement error which represent a fundamental limit.

We can thus conclude that in this particular case, frequency stress is a very good way to improve the accuracy of this fully digital alternate test. On the contrary, power supply stress does bring some information but in a much less significant extent. From a diagnosis viewpoint, we can legitimately assume that the modulator is much more limited dynamically than statically.

C. RF domain: Alternate test of a LNA through digital envelope signatures

A set of 200 instances of the LNA under test were obtained by electrical Monte Carlo simulation. Out of the 200 instances 150 were used to train the ensemble model, while 50 randomly chosen instances were taken apart as test set to verify the accuracy of the prediction. Model training was performed firstly under nominal conditions, and repeated in the different stressed scenarios as explained in the previous section. The supply voltages of LNA and envelope detector (labelled V_{DD} and V_{DDRect} in Fig. 3, respectively) are connected together in all the simulations.

Fig. 7 shows the scatter plots of the estimated versus measured Gain, NF, and 1dB compression point obtained for the test set when training the models with the original test signatures (circles), and for the complete set of test signatures with supply stress (triangles). Again, the prediction models are clearly improved when multi-condition operation is considered. The model FOM, registered in Table I, increases a 66% for Gain estimations, a 20% for NF estimations, and a 34% for 1dB compression point estimations.

V. Conclusions

Alternate test is undoubtedly an interesting path to mitigate the ever increasing cost of testing embedded analog, mixed-signal and RF blocks. In this paper, we have presented a simple technique, based on varying the operating conditions of the DUT, to improve the quality of alternate test techniques. It has the potential to improve many existing test strategies at a very low cost. As practical examples of application, the proposed

TABLE I
MODEL FOM IN THE DIFFERENT REGRESSION SCENARIOS

		Nominal	supply stress	frequency stress	supply + frequency stress
Predictive OBT	FOM(THD)	1.80	2.59	3.43	3.88
	Improvement	—	+44%	+91%	+116%
$\Sigma\Delta$ modulator digital test	FOM(SNDR)	8.4	9.1	17.1	17.3
	Improvement	—	+8.3%	+104%	+106%
Envelope-based test of LNAs	FOM(Gain)	3.49	5.81	—	—
	Improvement	—	+66%	—	—
	FOM(NF)	2.72	3.24	—	—
	Improvement	—	+20%	—	—
	FOM(CP1dB)	3.63	4.88	—	—
	Improvement	—	+34%	—	—

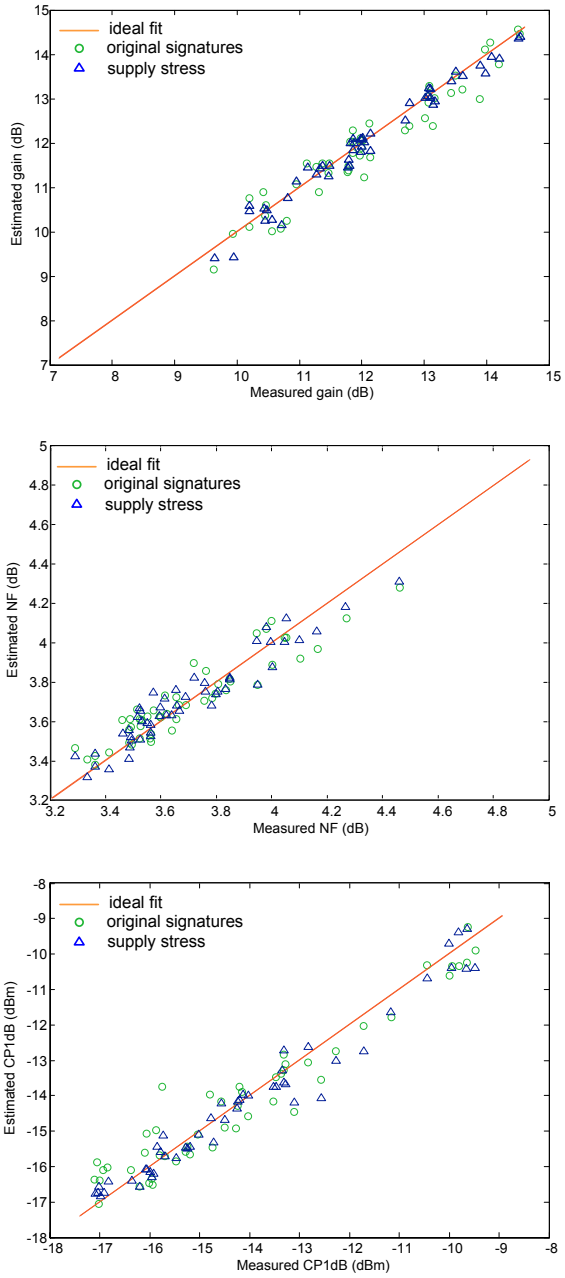

Fig. 7. Scatterplot of the regression results over the independent test set

methodology has been successfully applied to analog, mixed-signal and RF test schemes achieving a significant improvement of the mapping models for the considered specifications.

ACKNOWLEDGMENT

Authors want to thank Rafaella Fiorelli for her assistance in RF design. This work has been partially funded by a CSIC JAE-Doc contract (cofinanced by FSE), the Junta de Andaluca project P09-TIC-5386, the Ministerio de Economia y Competitividad project TEC2011-28302, both of them co-financed by the FEDER program, and Catrene project TOETS ($CT302$).

REFERENCES

[1] R. Voorakaranam, S. S. Akbay, S. Bhattacharya, S. Cherubal, and A. Chatterjee, "Signature testing of analog and rf circuits: Algorithms and methodology," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, no. 5, pp. 1018 –1031, may 2007.

[2] M. Barragan, R. Fiorelli, G. Leger, A. Rueda, and J. Huertas, "Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs," in *Proc. of IEEE Asian Test Symposium, Accepted for publication*, 2011.

[3] G. Huertas, D. Vazquez, E. Peralias, A. Rueda, and J. Huertas, "Practical oscillation-based test of integrated filters," *Design Test of Computers, IEEE*, vol. 19, no. 6, pp. 64 – 72, nov/dec 2002.

[4] G. Leger and A. Rueda, "Low-Cost digital detection of parametric faults in cascaded $\Sigma\Delta$ modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1326–1338, 2009.

[5] M. J. Barragan, R. Fiorelli, G. Leger, A. Rueda, and J. L. Huertas, "Alternate test of LNAs through ensemble learning of on-chip digital envelope signatures," *Journal of Electronic Testing*, vol. 27, no. 3, pp. 277–288, 2011.

[6] E. Silva, J. Pineda de Gyvez, and G. Gronthoud, "Functional vs. multi-VDD testing of RF circuits," in *Proc. of IEEE International Test Conference ITC*, 2005.

[7] P. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 2, pp. 349–361, March 2002.

[8] A. Raghunathan, H. J. Shin, J. Abraham, and A. Chatterjee, "Prediction of analog performance parameters using oscillation based test," in *Proc. of the IEEE VLSI Test Symposium*, april 2004, pp. 377 – 382.

[9] J. D. Wichard, M. J. Ogorzalek, and C. Merkwirth, "Entool-a toolbox for ensemble modelling," in *Europhysics Conference Abstracts ECA*, vol. 27, 2003.

[10] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 50, no. 3, pp. 352–364, 2003.